Incremental Data Converters

Gabor C. Temes[1] , Yan Wang[2] ,Wenhuan Yu[3] and Janos Markus[4]
[1]School of EECS, Oregon State University, Corvallis, OR,USA
[2]Texas Instruments, Tucson, AZ, USA
[3]Silicon Labs, Austin, TX, USA
[4]Robert Bosch Kft, Budapest, Hungary

Abstract - **Incremental data converters (IDCs) are high-accuracy oversampled analog-to-digital converters (ADCs). They form a special subclass of the commonly used delta-sigma ADCs. Unlike the latter, IDCs are only operated intermittently, typically for a few hundred clock periods, and hence they possess only a finite memory. They offer advantages in high accuracy, stability, absence of idle tones, low power dissipation, and ease of multiplexing. Hence, they are often used in sensor and MEMS interfaces.**

In this paper, some recent results on the theory and design of IDCs are discussed, and illustrated with the description of a recently implemented data converter.

I. Introduction

Delta-sigma (ΔΣ) ADCs are commonly used in communication and consumer electronics. They offer excellent waveform conversion accuracy, combined with low sensitivity to the non-ideal effects in the analog circuitry. However, they are not always suitable for instrumentation and measurement (I&M) applications, where high sample-by-sample conversion accuracy is required, and where offset and gain errors are not tolerated. By using the ΔΣ ADC intermittently to derive the digital equivalent of a sampled-and-held input signal, high absolute accuracy can be obtained with low power dissipation. Also, the ADC can easily be multiplexed among several channels, which may be a useful feature in some biomedical sensor systems such as electroencephalographic (EEG) and electrocardiogram (ECG) systems [1]. Analog-to-digital (A/D) converters with high SNDR are needed in these applications. Due to the nature of the input signals and sensor systems (low frequency and multiple channels), the multiplexed incremental ADC [2] is a good candidate for the task.

As shown in Fig. 1, the incremental ADC is a delta-sigma ADC which is reset periodically. Between two resets, the decimation filter provides the conversion result. After each reset, the incremental ADC can be switched to convert the signal in the next channel. In this way, a single incremental ADC can easily be time-multiplexed between many channels.

In this paper, some recent results are described on the theory and design of incremental data converters.

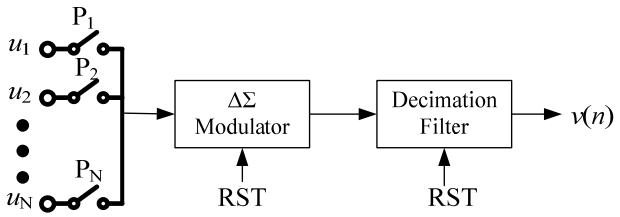

Fig. 1. Block diagram of a multiplexed incremental ADC.

II. Optimal Decimation Filter For Incremental ADCs

As shown in Fig. 2, a cascade of integrators can be used as the decimation filter for incremental ADCs [2]. However, such filter is not optimal for suppressing the combination of quantization and thermal noises [3].

As shown in Fig. 3, the incremental ADC is reset every M clock periods. The final result after the nth conversion cycle is given by

$$v(n) = \left[stf'(k) * u(k)\right]_{M,n} + \left[stf'(k) * t(k)\right]_{M,n} + \left[ntf'(k) * q(k)\right]_{M,n} \quad (1)$$

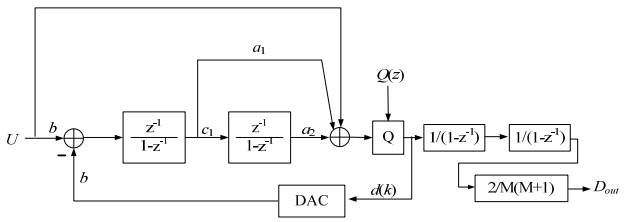

Fig. 2. An incremental ADC with cascaded integrator decimation filter.

where $stf'(k)$ is the M-sample long impulse response of the overall signal transfer function $STF(z)H(z)$, and $ntf'(k)$ is the M-sample long impulse response of the overall noise transfer function $NTF(z)H(z)$. Here, $STF(z)$ and $NTF(z)$ are the signal and noise transfer functions of the ΔΣ modulator without reset, respectively. $H(z)$ is the transfer function of the decimation filter without reset, $u(k)$ is the input signal, $t(k)$ is the input-referred thermal noise and $q(k)$ is the quantization noise.

ISBN 978-963-311-370-7

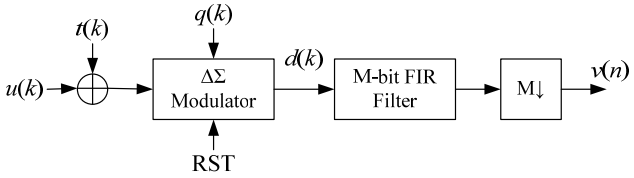

Fig. 3. Noise analysis of the incremental ADC.

Based on eq. (1), it is possible to optimize the decimation filter to minimize the total output noise (quantization and thermal noise) for given M and C_{in} (input sampling capacitor of the first integrator) by solving a quadratic program [3]. As an illustration, for the ADC reported here in Sec.VII, after a series of optimizations for different M and C_{in}, we found M = 230 and C_{in} = 2 pF as the optimal design parameters. The impulse response of the optimal decimation filter is shown in Fig. 4.

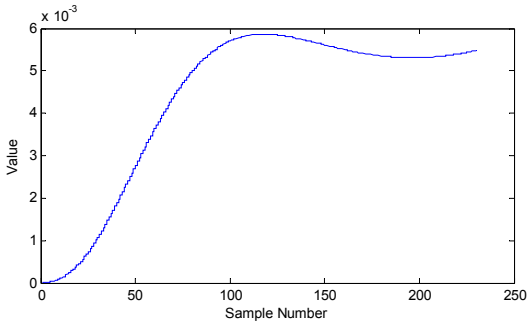

Fig. 4. The impulse response of the optimal decimation filter.

III. Comparison Between ΔΣ and Incremental ADCs

It can be shown that the output quantization noise after decimation is approximately proportional to $1/M^{2L+1}$ for an Lth order ΔΣ ADC, and is approximately proportional to $1/M^{2L}$ for an Lth order incremental ADC [2].

The performance degradation of incremental ADC is the price for the ability to multiplex between multiple input channels. Because of the reset of ΔΣ modulators and decimation filter, the length of the impulse response of the NTF for an incremental ADC is limited to M samples. Therefore, incremental ADCs usually have lower SQNR than their ΔΣ counterparts.

This handicap is illustrated by the peak SQNR versus OSR graph (Fig. 5) for a second-order ΔΣ ADC with a sinc^3 decimation filter, as well as for a second-order incremental ADC with a cascaded integrator decimation filter, and for a second-order incremental ADC with an optimal decimation filter.

IV. Noise-Coupled Incremental ADCs

Noise-coupling technique has been applied to different ΔΣ ADCs [4-6]. Fig. 6 shows the general block diagram of a noise-coupled incremental ΔΣ modulator. The adder output is

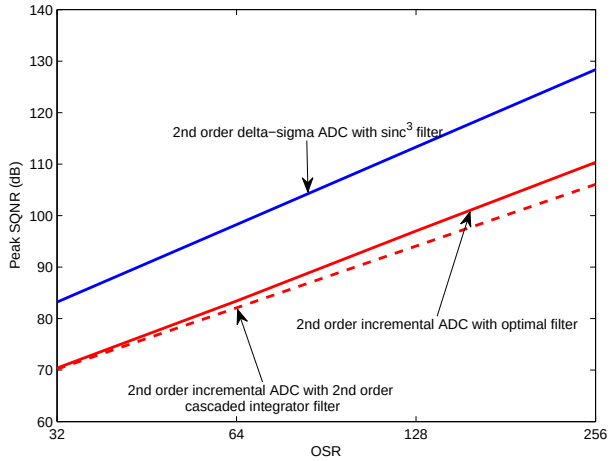

Fig. 5. Peak signal-to-quantization-noise ratio (SQNR) versus over-sampling ratio (OSR) for ΔΣ ADCs and incremental ADCs.

the linear combination of the loop filter output and the previous value of the quantization noise:

$$Y(z) = [U(z) - V(z)]H(z) - z^{-1}E(z) \qquad (2)$$

For the design of proposed noise-coupled incremental ΔΣ modulator, an estimate of $y(n)$ (and hence $Y(z)$) is required. For a DC or low frequency input signal, the modulator input U(z) and output V(z) are both known. Therefore, the first term of (2), Y_1 (z), can be easily calculated from the designed loop filter transfer function H(z). However, the second term contains the quantization noise, and cannot be numerically extracted to estimate the adder output voltage Y(z).

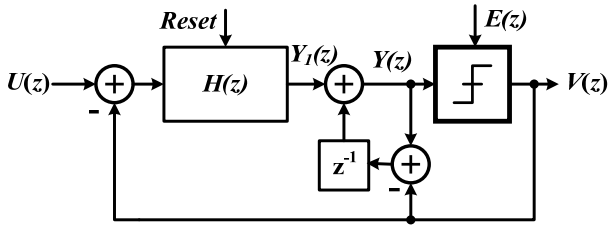

Fig. 6. Block diagram of the noise-coupled incremental ΔΣ modulator .

To make the numerical estimation of Y(z) possible, the adder output Y(z) should be only determined by the deterministic signals, $U(z)$ and $V(z)$ of the modulator, which means the simplified equivalent model should be derived. As shown in Fig. 7(a), the adder with noise-coupling can be spilt into two input branches, one from Y_1(z) and the other one-cycle delayed V(z), followed by a local feedback loop whose transfer function is equal to that of a delay-free integrator. A more detailed behavior model is thus that in Fig. 7(b), and the adder output is the sum of Y_{1a}(z) and Y_{2a}(z):

$$Y_{1a}(z) = Y_1(z)\frac{1}{1-z^{-1}} \qquad (3)$$

$$Y_{2a}(z) = V(z)\frac{z^{-1}}{1-z^{-1}} \tag{4}$$

Therefore,

$$Y(z) = \frac{H(z)}{1-z^{-1}}U(z) - \frac{H(z)+z^{-1}}{1-z^{-1}}V(z) \tag{5}$$

For a given noise-coupled incremental ΔΣ modulator, the input signal $U(z)$, modulator output $V(z)$ and the loop filter transfer function $H(z)$ are all known, so the adder output at the end of M cycles can be readily calculated from the preset initial conditions of the system, which can be assumed all zero. This is used below to derive the decimation filter transfer function.

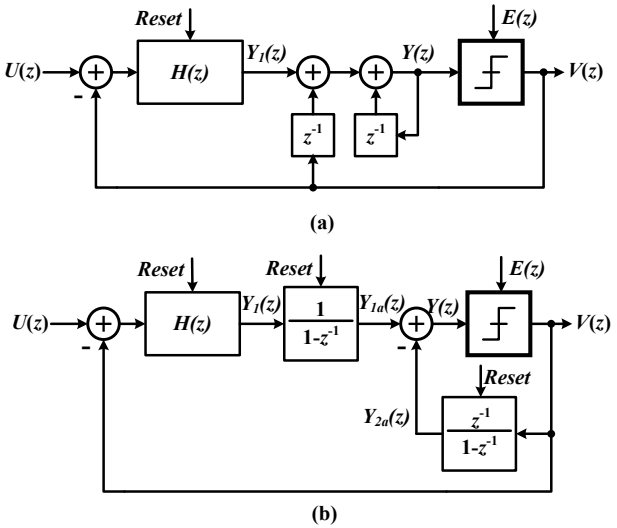

Fig. 7. Equivalent models of a noise-coupled incremental ΔΣ modulator.

V. Noise-Coupled IDC Design Example

To verify the validity of the proposed architecture, a noise-coupled incremental ΔΣ modulator was designed for a biomedical application. To simplify the discussion, a single-channel input signal was considered. The key design specifications are summarized at Table 1.

TABLE I. Design Specification of the Incremental ΔΣ ADC

Design Parameters	Design Specifications
Signal Bandwidth	>1kHz
Oversampling Ratio	<128
Quantizer bits	1bit
Conversion Resolution	>16bit
Power Dissipation	<10uA/channel

For the incremental ADC design, the conversion accuracy is usually affected by different noise sources, such as the wideband thermal noise, low frequency flicker noise and the quantization noise. Using chopping and correlative-double sampling (CDS) techniques, most of the flicker noise can be effectively cancelled. Also, for low power design it is desirable to make the noise floor dominated by the thermal noise, which means that the conversion error due to quantization noise should be negligible. In this application, more than 20 bit signal-to-quantization noise ratio (SQNR) is targeted. Since the oversampling ratio was limited up to 128 for low power dissipation, a single-loop second-order incremental ADC could not fulfill the design requirements. To increase the conversion accuracy, and at the same time maintain good stability of the loop, an extended counting structure is used. Fig. 8 shows the proposed architecture. For the first-stage ΔΣ loop, a first-order modulator with noise-coupling technique was used. So, effectively a second-order noise-shaping is achieved. By adding a direct input branch to the quantizer, the signal transfer function of the modulator becomes equal to 1. So, the integrator only needs to deal with the random noise and its linearity requirement is greatly relaxed. Under normal operation, the modulator periodically processes the input signal for 128 clock cycles, and then resets for the next input sample conversion. Based on the discussion in Section IV, the adder output voltage $y(M)$ after M clock cycles is the integration result for the input signal and modulator output bit sequence v(k). Assuming a DC input voltage, y(M) can be written as

$$y(M) = \sum_{l=1}^{M}\sum_{k=0}^{l-1} u + \sum_{k=1}^{M} u - \sum_{l=1}^{M}\sum_{k=0}^{l-1} v(k) - \sum_{k=0}^{M-1} v(k) \tag{6}$$

If the modulator is stable, y(M) is a bounded value. So, if M is large enough, the estimation of input signal u is

$$u \approx \frac{2}{M(M+1)}\sum_{k=0}^{M-1}(M+1-k)v(k)\,|_{M=128} \tag{7}$$

The estimation error is

$$e_{y[M]} = \frac{2}{M(M+1)}y(M) \tag{8}$$

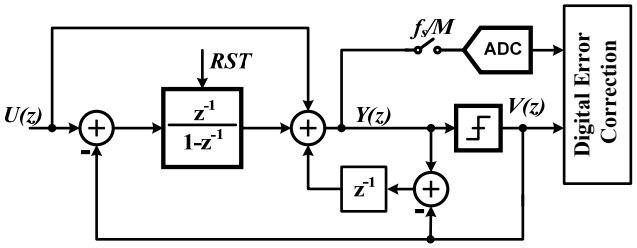

Fig. 8. The noise-coupled IDC using an extended counting structure.

To further reduce $e_{y[M]}$, the adder output is further sampled at the end of each conversion cycle, and then digitized by another power-efficient successive approximation (SAR) ADC. Using digital error correction logic, the quantization error in the overall output originates ideally only from the quantization error in the SAR ADC:

$$e_{Q-ADC} = \frac{2}{M(M+1)}e_{Q-SAR} \tag{9}$$

So, if a high resolution SAR ADC is used, the residue quantization error can be greatly reduced.

Eq. (7) gives the estimated value of the input signal as the convolution of the modulator output sequence $v(k)$ and the impulse response of a decimation filter $H_{DEC}(z)$, whose transfer function is

$$H_{DEC}(z) = \frac{2}{M(M+1)} \sum_{k=0}^{M-1} (k+1) z^{-k} \qquad (10)$$

The magnitude response of $H_{DEC}(z)$ is plotted in Fig. 9.

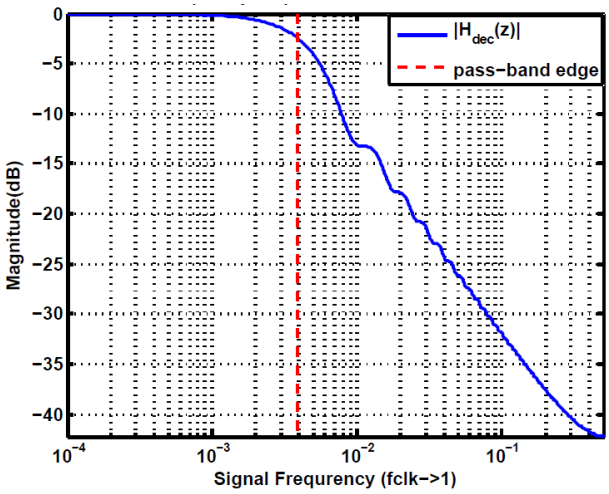

Fig. 9. Magnitude response of the decimation filter.

So, the decimation filter has the zero dB output gain at dc and decreases with increased frequency. For OSR=128, the gain drop at the edge of signal band is around -2.5dB, so input signal is attenuated at the incremental ADC output. But it can be easily compensated with following digital signal processor.

The overall ADC performance has been evaluated using Matlab simulations. To check the incremental ADC conversion accuracy for a dc input signal, the full-range input voltage is swept. The resolution of additional SAR ADC is set to 6 bits.

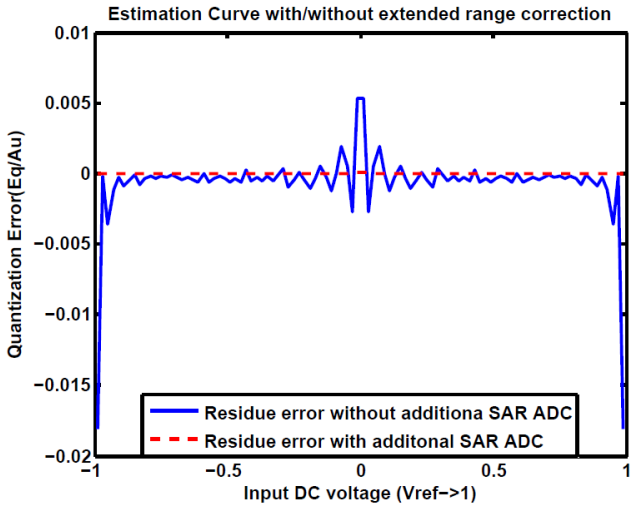

Fig. 10. The relative quantization error before/after extended counting.

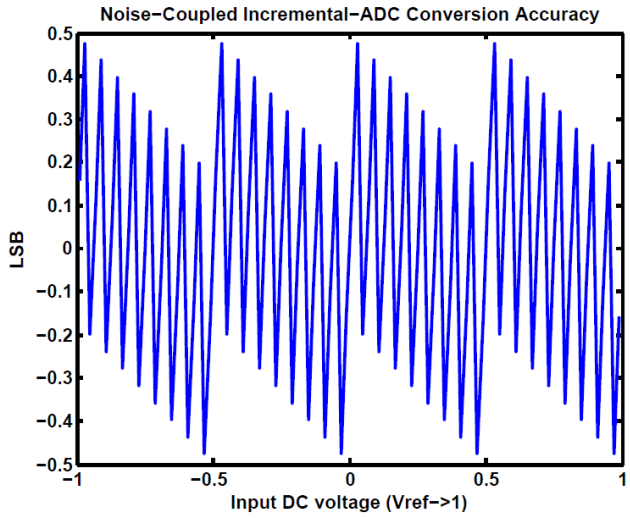

Fig. 11. Conversion error of the IDC.

Fig. 10 shows the relative quantization error, scaled to each input amplitude Au, before and after applying the extended counting. Large improvements have been achieved. The absolute conversion accuracy due to quantization error with extended counting is also plotted at Fig. 11, in which one LSB stands for 20 bit accuracy. Therefore, with 2nd order noise-shaping, OSR=128 and single-bit quantizer, 20-bit accuracy can be achieved with an additional 6-bit SAR ADC.

With a -2.5dB, 500Hz sinusoidal input signal, the simulated output spectrum is shown in Fig. 12. With ideal analog blocks, SQNR is 119.1dB. So, for the AC signal, around 19.5 bit conversion accuracy due to quantization error can still be achieved.

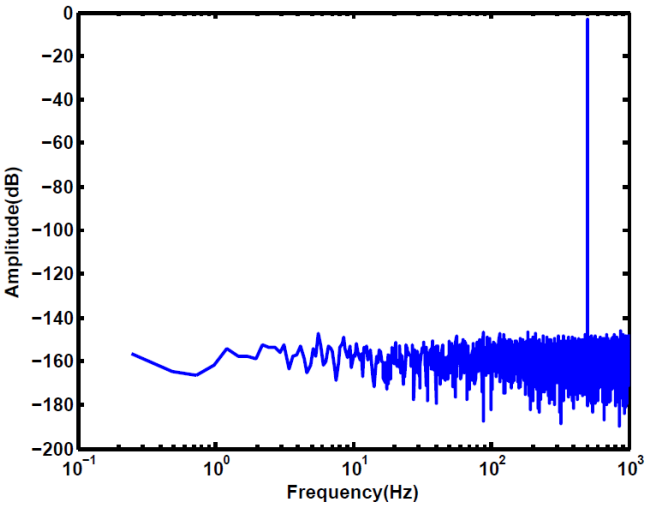

Fig. 12. Simulated output spectrum.

VI. DAC Mismatch Calibration And Correction

For IDCs with multi-bit internal quantizer, the mismatch errors between DAC elements need to be corrected or filtered out of the signal band.

To obtain the mismatch of the DAC elements, a dummy calibration capacitor is added in the first integrator of a third-order ΔΣ modulator [7] (Fig. 13). Four capacitors are used in the DAC to feed the 5-level quantizer output back to the input. The input and DAC feedback capacitors are shared.

A log shifter is added after the quantizer. This log shifter, similar to that in DWA, shifts the quantizer output (in thermometer code) according to a pointer. However, in the calibration mode, the pointer is controlled by an off-chip signal (DACPTR1 and DACPTR0 pins), instead of by a DWA logic.

In the calibration mode, the ΔΣ modulator is run as an incremental ADC. Four conversions are needed to obtain the DAC mismatch information. In each conversion, the PTR (DACPTR1 and DACPTR0) sets one of the DAC capacitors as the first DAC element.

Let $C_i = C(1 + x_i)$, $i = 1, 2, 3, 4$, where C_i is the value of the DAC element capacitor and C is the value of the calibration capacitor. We regard C as the desired value of the DAC element capacitors. The x_i ($i = 1, 2, 3, 4$) are the relative DAC mismatch errors. In the calibration mode, we connect the input terminal to the common-mode voltage, and the calibration capacitor branch to VREF+. Effectively, we are applying an input voltage Vref / 4.

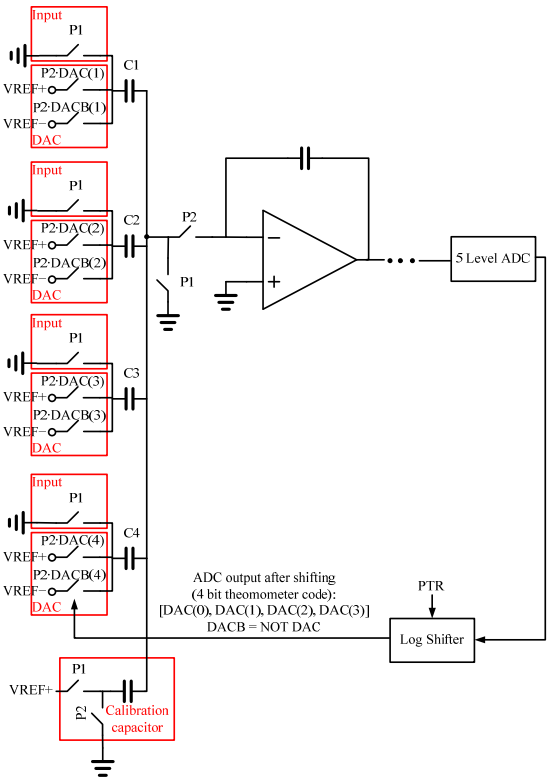

Fig. 13. The DAC and calibration capacitor in the first integrator.

It can be shown that by setting the parameter PTR to 0, and then to 1, 2 and 3, we obtain

$$\begin{bmatrix} \frac{1}{4} & \frac{1}{4} & \frac{1}{4}a_1 & -\frac{1}{4} \\ -\frac{1}{4} & \frac{1}{4} & \frac{1}{4} & \frac{1}{4}a_2 \\ \frac{1}{4}a_3 & -\frac{1}{4} & \frac{1}{4} & \frac{1}{4} \\ \frac{1}{4} & \frac{1}{4}a_4 & -\frac{1}{4} & \frac{1}{4} \end{bmatrix} \begin{bmatrix} x_1 \\ x_2 \\ x_3 \\ x_4 \end{bmatrix} = \begin{bmatrix} b_1 \\ b_2 \\ b_3 \\ b_4 \end{bmatrix}. \quad (11)$$

where a_i and b_i (i =1, 2, 3, 4) are calculated from the modulator output [7]. Solving (2) gives the DAC mismatches. After the DAC mismatches are obtained, they can be compensated with a look-up table in the digital domain. Since the transfer function of the DAC mismatch errors is approximately 1 in the signal band, we can simply subtract the DAC mismatch errors from the quantizer output.

The proposed DAC calibration and correction technique can be used in the double-sampling scheme, to reduce the noise-folding problem caused by the mismatch between the two DACs operating in opposite phases. The DWA is not effective in solving the noise-folding problem.

VII. Implementation Example

To confirm the theoretical results discussed above, a low-distortion third-order single-loop delta-sigma modulator with a 5-level quantizer (Fig. 14) was designed and fabricated. It consists of three integrators, a passive adder, a 5-level quantizer with pre-amplifier, comparator latches, DWA logic, output drivers, a clock generator and the biasing circuit.

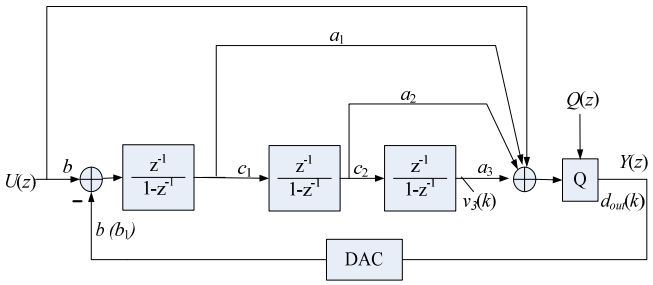

Fig. 14. Block diagram of the 3rd-order ΔΣ modulator.

As shown in Fig. 15, chopping was used in the first integrator to reduce the 1/f noise of the OTA. A special fractal chopping sequence (1, −1, −1, 1, −1, 1, 1, −1) was used for better performance [2]. The input and feedback DAC capacitors are shared. The input common-mode voltage of the OTA was set to 0.3 V, and the output common-mode voltage to 0.9 V.

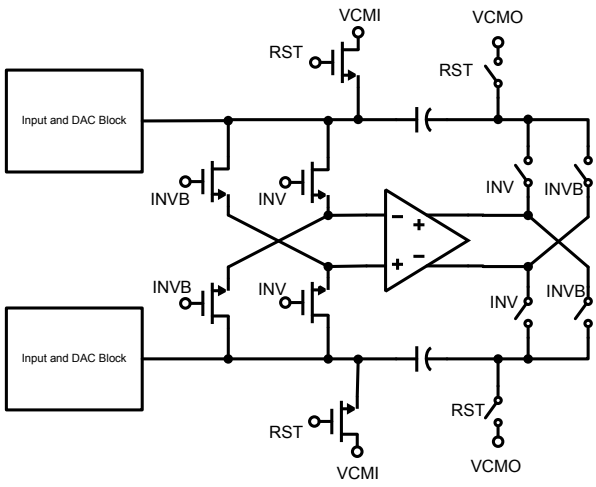

Fig. 15. The first integrator with chopping.

VI. Measurement Results

The prototype was fabricated in a double poly/6-metal 0.18 µm CMOS process. The total power consumption is 6.6 mW (3.8 mW for the analog circuitry, and 2.8 mW for the digital).

The spectra of the incremental ADC output after decimation, with both the optimal decimation filter and the traditional cascaded-integrator one, are shown in Fig. 16. For a −3.4 dBFS sine wave input, the SNR is 83.7 dB and the SNDR 81.5 dB with the optimal decimation filter, and SNR = 82.3 dB, SNDR = 79.7 dB with the cascaded integrator decimation filter. The sampling frequency was 10 MHz.

Fig. 17 illustrates the effectiveness of the digital calibration for the circuit used as a ΔΣ modulator. With digital compensation, it achieves 80.1 dB SNR and 73.4 dB SNDR, while without digital compensation only 71.3 dB SNR and 63.6 dB SNDR. Thus, around 10 dB improvement is obtained by digital compensation and calibration.

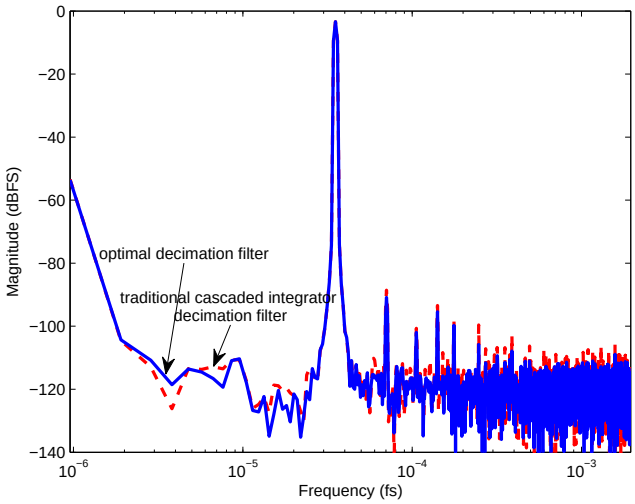

Fig. 16. The spectrum of the incremental ADC output (after decimation) with the optimal decimation filter (solid line) and the traditional cascaded integrator decimation filter (dashed line).

The performance of the incremental modulator is summarized in Table II. The die micrograph is shown in Fig. 18.

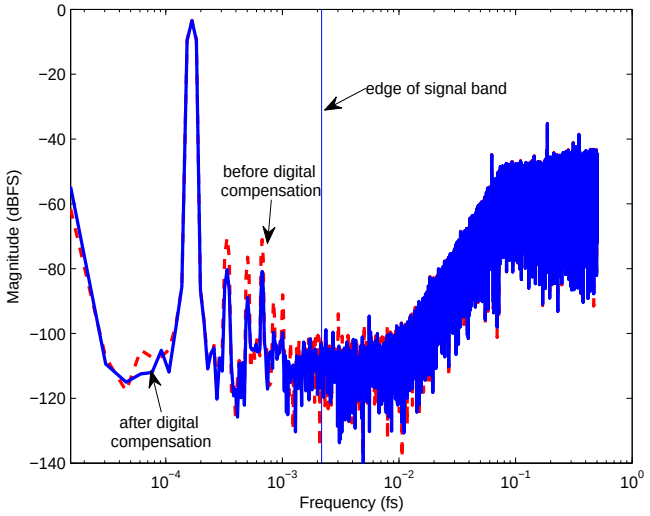

Fig. 17. The spectrum of the modulator output (the modulator is running as a conventional continuously-running ΔΣ modulator) before (dashed line) and after digital compensation (solid line). The DWA is turned off.

VII. Conclusion

An incremental ADC with a novel digital calibration, fractal chopping, and optimal decimation filter was designed and fabricated in 0.18 µm CMOS process. The theoretical results and the optimization technique were verified by the measurement results. The digital calibration improved the SNDR performance by 10 dB, while the use of the optimal decimation filter by about 2 dB.

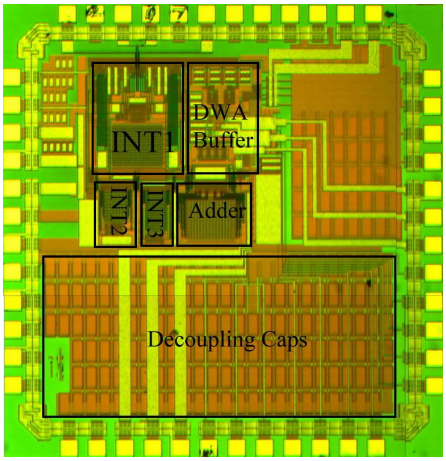

Fig. 18. Die micrograph of the incremental ADC.

TABLE II. Performance Summary

Performance	Value
Sampling Frequency	10 MHz
Number of Channels	20
Signal Bandwidth	1.1 kHz
Oversampling Ratio	230
Peak SNR	83.7 dB
Peak SNDR	81.5 dB
Input Range	2 Vpp (differential)
Power Consumption	0.19 mW/channel (analog) 0.15 mW/channel (digital)
Power Supply	1.8 V
Process	0.18 μm CMOS
Chip Area	6.25 mm^2 (core area: 1.2 mm^2)

ACKNOWLEDGMENTS

The authors are grateful to the National Semiconductor Corporation for funding this research and fabricating the chip.

REFERENCES

[1] G. Lantz et al., "Epileptic source location with high-density EEG: how many electrodes are needed?" *Clinical Neurophysiology*, 2003:114, pp.63-69.

[2] V. Quiquempoix, P. Deval, A. Barreto, G. Bellini, J. Márkus, J. Silva and G. C. Temes, "A low-power 22-bit incremental ADC," *IEEE Journal of Solid-State Circuits*, vol. 41, no. 7, pp. 1562–71, 2006.

[3] J. Steensgaard, Z. Zhang, W. Yu, A. Sárhegyi, L. Lucchese, D.-I. Kim and G. C. Temes, "Noise-power optimization of incremental data converters," *IEEE Trans. on Circuits and Systems I*, Jun. 2008.

[4] K. Lee, M. Bonu, and G. C. Temes, "Noise-coupled delta-sigma ADCs," Electronics. Lett., vol. 42, no. 24, pp. 1381-1382, Nov. 2006.

[5] K. Lee, J. Chae, M. Aniya, K. Hamashita, K. Takasuka, S. Takeuchi and G. C. Temes, "A noise-coupled time-interleaved ΔΣ ADC with 4.2MHz BW, -98dB THD and 79dB SNDR," *IEEE ISSCC Digest*, pp 494-495, Feb 2008.

[6] Y. Wang and G. C. Temes, "Noise-Coupled Continuous-Time Delta-Sigma ADCs," *Electronics Letters*, vol.45, pp 302-303, Mar. 2009.

[7] W. Yu and G. C. Temes, "A Digital Calibration Technique for DAC Mismatches in Delta-Sigma Modulators," *IEEE Int. Symp. on Circuits and Systems*, Taipei, Taiwan, 2009.